AMENDMENTS TO THE SPECIFICATION

Please replace paragraph beginning on page 5, line 21 with the following paragraph:

FIG. 1 is a schematic diagram illustrating use of a DC mitigation circuit in accordance with the first exemplary embodiment of the invention. FIG. 1 illustrates a single phase transformer 1 connected to an output filter 3, which is connected to a DC mitigation circuit 13. The single phase transformer 1 has a primary winding 15, a secondary winding 16 connected to a load 6, a tertiary winding 2 connected to the output filter 3, and a core 17. The output filter 3 contains a capacitor 5 and inductors 4 connected to the DC mitigation circuit 13. The DC mitigation circuit 13 contains an H-bridge rectifier 14 formed from four n channel metal-oxide semiconductor field-effect transistor (MOSFET) switches 10, (although p channel MOSFET switches may be substituted). The inductors 4 in the output filter 3 are each connected between a source and a drain of one of a pair of MOSFET switches 10 in the H-bridge rectifier 14. Each MOSFET switch 10 has an anti-parallel diode 12, *i.e.*, a diode connected across an electrical element such that current flow through the diode is opposite that through the element, connected across its source and drain. Power is supplied to the source of two MOSFET switches 10 and to the drain of the other two MOSFET switches 10 via capacitor 11.

Please replace paragraph beginning on page 7, line 23 with the following paragraph:

As is shown in FIG. 4, in order to perform primary compensation, the DC mitigation control circuit 7 is connected to the primary winding 15 of the transformer 1 at current sensor 9. The DC mitigation control circuit 7 first measures the amount of DC

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current in the primary winding, *e.g.*, via the Hall effect, as shown in block 20 of FIG. 4. Then, as shown by the multiplier block 21 and the ratio block 26, the DC mitigation control circuit 7 multiplies the measured DC current by the ratio of the number of turns of the primary winding 15 to the number of turns of the tertiary winding 2. The output of the multiplier block 21 represents the amount of DC current that is required to be generated by the tertiary winding 2 to offset the flux created by the DC current in the primary winding 15. The output of the multiplier block 21 is inputted to the summing block 22. The summing block 22 adds the output of the multiplier block (a positive value) to the output of the loop compensation block ~~26~~ 25, (*i.e.*, the value of the last DC current outputted by the H-bridge 24). The loop compensation block 25 inputs a negative value into summing block 22. If summing the input from the multiplier block 21 and the input from the loop compensation block 25 results in a zero value, then the DC mitigation circuit 13 is performing compensation correctly, and the H-bridge 24 maintains its current output. However, if the result output from the summing block 22 is not zero, then a signal indicating the amount of current necessary to offset the flux created by DC current in the primary winding 15 is amplified in block 23 and outputted to the H-bridge 24.

Please replace paragraph beginning on page 8, line 19 with the following paragraph:

As is shown in FIG. 5, in order to perform secondary compensation, the control circuit 7 is connected to the secondary winding 16 of transformer 201 at connection point 18 or alternatively to the primary winding 15 at connection point 9. As shown in block 30, the DC mitigation control circuit 7 of the instant invention first performs a harmonic current measurement using, for example, a Fast Fourier Transform on the input

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from either the secondary winding 16 or the primary winding 15. The control circuit 7 then outputs the magnitude and phase data generated in block 30 to a compensation network block 31. The compensation network block 31 determines the magnitude and phase the tertiary winding ~~12~~ 2 is required to output to offset that created by harmonic AC current in either the primary winding 15 or the secondary winding 16. The output of the compensation network block 31 (positive values) is then inputted into the summing block 32 along with the output of a loop compensation block 35 (*i.e.*, the magnitude and phase of the last current output by the H-bridge 34). Like primary compensation, the loop compensation block 35 outputs a negative value. Also like primary compensation, if the output of summing block 32 is zero, then the H-bridge 34 maintains its current output. However, if the summing block 32 outputs a non-zero value, then a signal indicating the current necessary to offset the harmonic AC is amplified in block 33 and then outputted to H-bridge 34.

Please replace paragraph beginning on page 11, line 5 with the following paragraph:

The DC current mitigation circuit 13 of the present invention may be tested using the simulated power system shown in FIG. 8. Either apparatus 300 or 301 was used to simulate injection of GICs into the transmission line 302 to determine the level of disruption GICs cause to a power system. Both apparatus 300 and 301 comprise a variable power source ~~304~~ and a capacitor ~~306~~ in parallel with transmission line 302. DC or harmonic currents resulting from the DC compensation was then provided by the present invention on a phase-by-phase basis. When the DC mitigation circuit of the instant invention was not employed, power quality degraded substantially. But, when the DC

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mitigation circuit was connected to the transformer, almost complete restoration of the baseline power quality was demonstrated.

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